ABSTRACT

The present invention relates to a digital bus system (1; 1a) of low power consumption. The bus system (1; 1a) is adapted to establish at least one parameter (M; M1) that indicates the number of transmitter units (9.1-9.N) in the bus system (1; 1a) which need to send data on a data bus (3). A clock signal (CLK2) that indicates a rate at which data is sent is generated with regard to the established parameter (M; M1) in accordance with a predetermined pattern. In this respect, the clock signal (CLK2) is generated in a manner such that the fewer the transmitter units (9.1-9.N) needing to send data, the lower the data rate on the data bus (3). This reduces the average power consumption of the transmitter units (9.1-9.N) and receiver (15). This lower power consumption is achieved without appreciably affecting waiting times in respect of transmitter units (9.1-9.N) being allowed to send data, since the clock signal (CLK2) is generated so that the data rate will be adapted in relation to the number of transmitter units (9.1-9.N) that need to send data.

Publication figure: Figure 1